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Etch Mechanisms

"Redeposition of Etch Products on Sidewalls during SiO2 etching in a fluorocarbon plasma. I. Effect of Particle Emission from the Bottom Surface in a CF_4 Plasma"
J.-H. Min, S.-W. Hwang, G.-R. Lee, S. H. Moon
J. Vac. Sci. Technol. A 20 (2002) 1574 - 1581

The effect of etch product re-deposition on vertical structures during the etching of SiO2 in a CF4 plasma was studied with a unique Faraday gage setup in a inductively coupled reactor. The use of the Faraday cage allowed the authors to scale up very small patterns because the mean free path of ions and radicals is larger than the height of the Faraday cage (distance between the grid of the Faraday cage and the bottom of the features. Various barrier plates and spacers were positioned within the Faraday cage to study the deposition on the sidewalls by reflectometry, FTIR, AFM, AES, and XPS. The results show the contribution of the layer formation by species emitted from the horizontal etch front. The sidewall deposition is comprised of C_xF_y type of polymers.

"Large Fluorocarbon Ions can Contribute to Film Growth During Plasma Etching of Silicon"
E.R. Fuoco, L. Hanley
J. Appl. Phys. 92 (2002) 37 – 44

In this study, mass selected 5 – 200 eV C_3F_5+ and C_2F_4+ ion beams were used to form nanometer thick fluorocarbon and $Si_xC_yF_z$ films on H-Si(100). XPS analysis shows that the average elemental and chemical content of the deposited film is nearly independent of ion identity and kinetic energy! The chemical nature of the fluorocarbon film is controlled by the surface chemical and diffusion processes. Ion energy and structure do control the fluorocarbon film morphology.

"In vacuo Electron-Spin-Resonance Study on Amorphous Fluorinated Carbon Films for Understanding of Surface Chemical Reactions in Plasma Etching"
K. Ishikawa, S. Kobayashi, M. Okigawa, M. Sekine, S. Yamasaki, T. Yasuda, J.-I. Isoya
Appl. Phys. Lett. 81 (2002) 1773 – 1775

An in vacuo electron-spin-resonance (ESR) technique was applied to study amorphous fluorinated carbon (a-C:F) films and their chemical reactivity with oxygen molecules. The experiments were carried out in a parallel plate reactor connected to an ESR system via a transfer system. The films were prepared in an Ar diluted c-C_4F_8 plasma at 10 Pa. The experimental results indicate that an a-C:F film has a characteristic property that is suitable for SiO2 etching. Because a-C:F is highly reactive with oxygen, it can easily react with oxygen in the underlying SiO_2 to increase the number of dangling bonds in the SiO_2.

Modeling of Plasma Etching

"The Role of Mask Charging in Profile Evolution and Gate Oxide Degradation"
K.P. Giapis, G.S. Hwang, O. Joubert
Microelectronic Engineering 61 – 62 (2002) 835 - 847

This paper reports on numerical simulations of the role of insulator mask thickness in altering the fidelity of pattern transfer and causing damage to buried gate oxides during plasma etching. It is found that the mask thickness changes the contact time of ions with the local electric fields, which can perturb the ion trajectories leading to sidewall bowing and microtrenching. For very thick

masks (as used for instance in deep trench etching), the simulations reveal an ion focusing effect due to significant charging of the mask sidewalls. This charging is shown to influence the shape of the etch front (bottom of the trench). Regarding gate oxide damage, it is shown that it is more likely observed for intermediate mask thickness values.

"Semiempirical Profile Simulation of Aluminum Etching in a Cl_2/BCl_3 Plasma"
D.J. Cooperberg, V. Vahedi, R.A. Gottscho
J. Vac. Sci. Technol. A 20 (2002) 1536 – 1556

A semiempirical profile simulator to predict the topography evolution of PR patterned Al during Cl_2/BCl_3 etching is presented. Angular and energy distributions and the etch yield as a function of incoming energy and angle are derived from experimental results (physical sputtering and ion enhanced etching). The spontaneous etch rate of Al by chlorine and the spontaneous desorption rates are also derived from specially devised experiments. Sticking coefficients and depositing fluxes are derived by fitting simulated to measured profiles. The calibration of the profile simulator by experimental results is described. The experimental data and the calibrated profile simulator are fed back to the plasma reactor model. Quantitative agreement with the hybrid plasma equipment model (HPEM by M. Kushner. University of Illinois) could be shown. The role of BCl_3 is not considered in the model.

Devices

How Small Can MOSFETs Get ?"
L. Risch
Advances in Microelectronic Device Technology, Proceedings of SPIE vol. 4600 (2001) 1 - 9

For future CMOS technology nodes, performance degradation is a big issue. 25 nm CMOS seems to feasible using very thin silicon substrates on insulator. Further improvements down to 10 nm are likely with two gates for the control of the charge carriers. When comparing double gate devices with SOI transistors, simulations show that the V_t roll off can be suppressed till 20 nm gate length for SOI, whereas double gate devices behave well down to 5 nm. The challenge for double gate transistors will be to develop a reliable process with self aligned gates. Tunneling from source to drain will set an end to the reduction of the channel length below 5 nm.

"Effects of Microtrenching from Polysilicon Gate Patterning on 0.13 μm MOSFET device performance"
C.S. Chua, E.F. Chor, J. Yu, Y. Pradeep, L. Chan
Proceedings of ISIC-2001, pp. 461 – 464.

Microtrenching has been shown to occur on the periphery of the isolated poly-Si line and the outmost edge of the nested lines first. This is explained by the restricted angle of incoming ion flux for the nested lines (the effect of etch rate microloading is not discussed). TSuprem4 and Medici simulations are carried out to evaluate the impact of microtrenching on device performance for a 0.13 μm NCOM transistor with a lightly doped drain (LDD) depth of 500 Å. Minor microtrenching (depth less than LDD depth) does not degrade the device performance significantly.

"Silicon Gate Notching for Patterning Features with Dimensions Smaller than the Resolution of the Lithography"
J. Foucher, G. Cunge, L. Vallier, O. Joubert
Microelectronic Engineering 61 – 62 (2002) 849 - 857

The design of a notched gate process is discussed. Details of the sidewall passivation layer engineering are given. A CF_4 breakthrough is followed by a traditional $HBr/Cl_2/O_2$ main etch. The bottom portion of the profile is etched anisotropically with passivation free gate sidewalls and stopped 10 nm above the gate oxide (Cl_2/SF_6 is demonstrated as an example for a chemistry that

forms a $SiCl_xF_y$ sidewall layer that does not act as a stopping layer for isotropic attack during subsequent steps. Notching is achieved during the HBr based overetch step. It is shown that this technique is limited by dense – iso microloading for gates below 100 nm and by the strong effect of chamber wall conditioning during the notching step which impacts negatively the across wafer CD uniformity as well as wafer to wafer repeatability.

"Poly-Si Gate Patterning Issues for Ultimate MOSFET"
D. Louis, M.E. Nier, C. Fery, M. Heitzmann, A.M. Papon, S. Renard
Microelectronic Engineering 61 – 62 (2002) 859 - 865

This paper describes sub 50 nm gate pattering by oxide hardmask trimming in a 1 % HF solution after mask open.