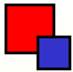
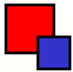


Etching for Nano-devices

J. Foucher, X. Detter, E. Pargon, N. Posseme: Ph D students

G. Cunge, T. Chevolleau, L. Vallier, O. Joubert: CNRS-LTM



Context

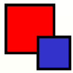
Plasma Etching: key technological step for IC miniaturisation

Plasmas are directly involved in miniaturisation through a controled erosion of the mask or gate materials

The fabrication of very small structures using plasmas reveal new unexpected problems: CD control is the major challenge

Strong R&D effort for advanced process control (Most etching processes must be controlled in real time)

New dielectric materials (low k and high k) bring new interesting issues for plasma etching



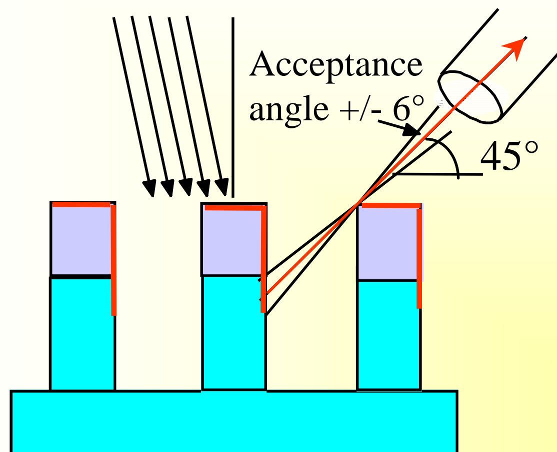
Experimental Platform

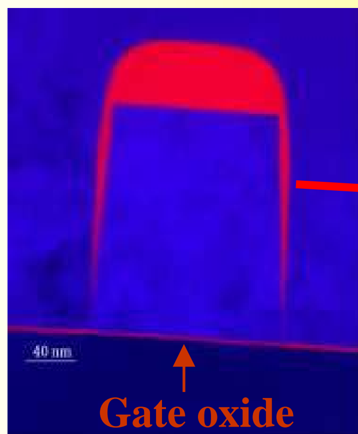
Modified industrial etching platform

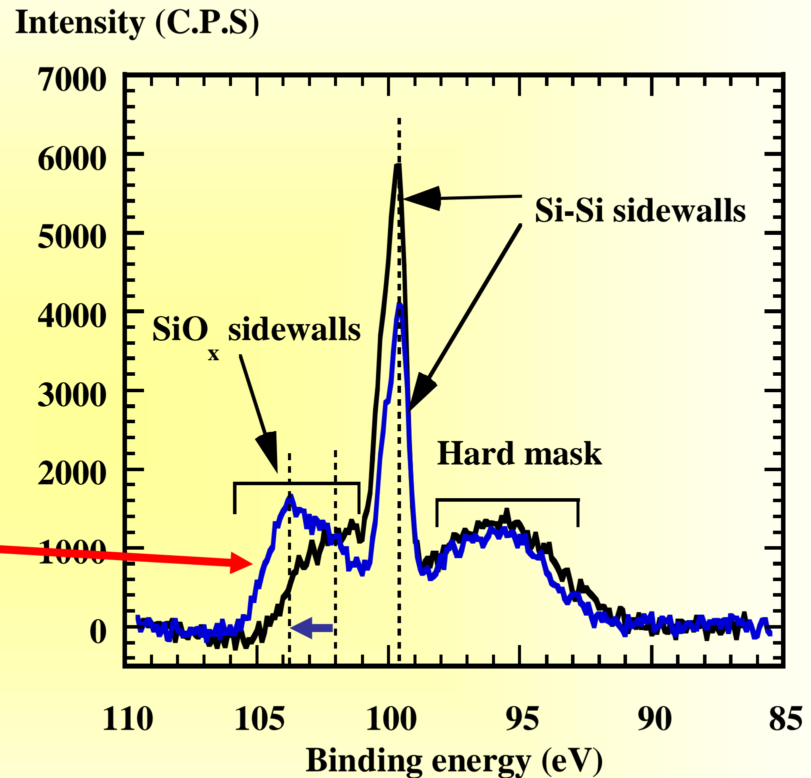
-Reliability and performance of an industrial system

-Transformed in a very powerful research tool for advanced process development

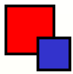
Chemical topography analyses of small structures by XPS







Understanding the formation mechanisms of passivation layers which control the etch profile is fundamental to design robust etch processes



Analyses of the species present in the plasma

Source rf power
12.56 MHz

Monochromator
Hg Lamp

Al_2O_3 dome

Ellipsometer

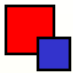
Optical emission and absorption

Bias rf power
13.56 MHz

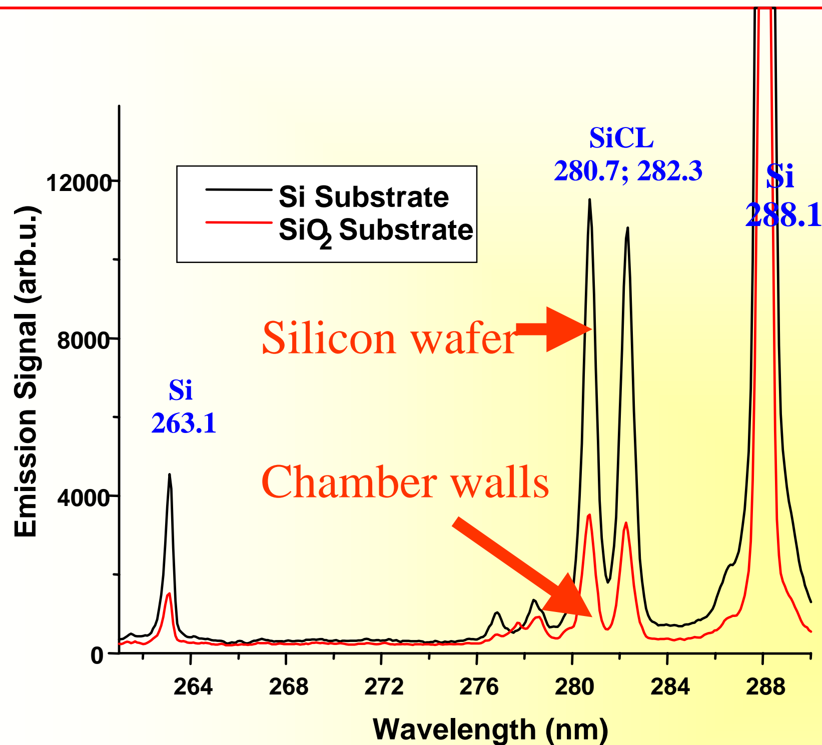
ESC Chuck
(200 mm wafers)

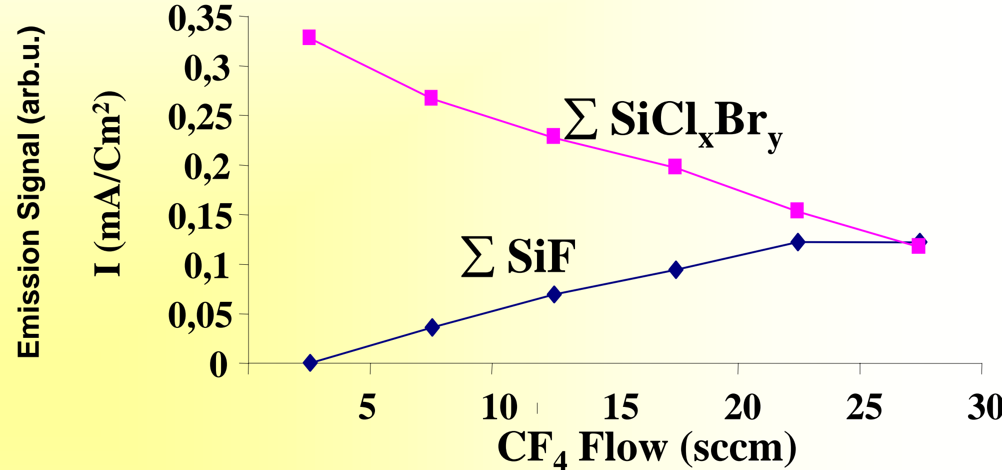
Mass spectrometer

Diagnostics of the plasma gas phase used to evaluate:
- the concentrations of the active species involved in the process
- the role of chamber walls on process stability



Monitoring of chamber walls cleanliness

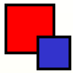




Optical emission: Impact of chamber walls cleanliness on process performance (reproducibility and control)

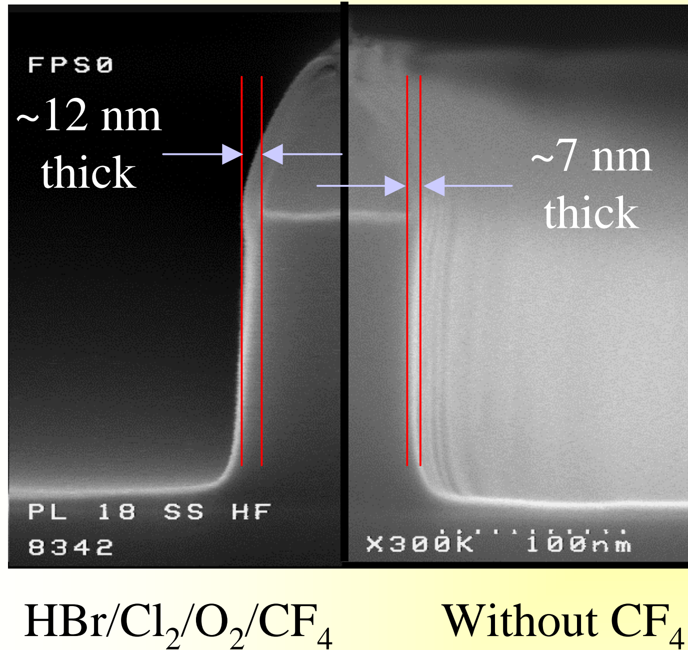
Mass spectrometry: impact of chemistry on ion flux composition and chamber walls stability

Chamber wall stability is a critical parameter directly impacting the design of plasma processes dedicated to the fabrication of nanostructures

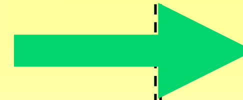


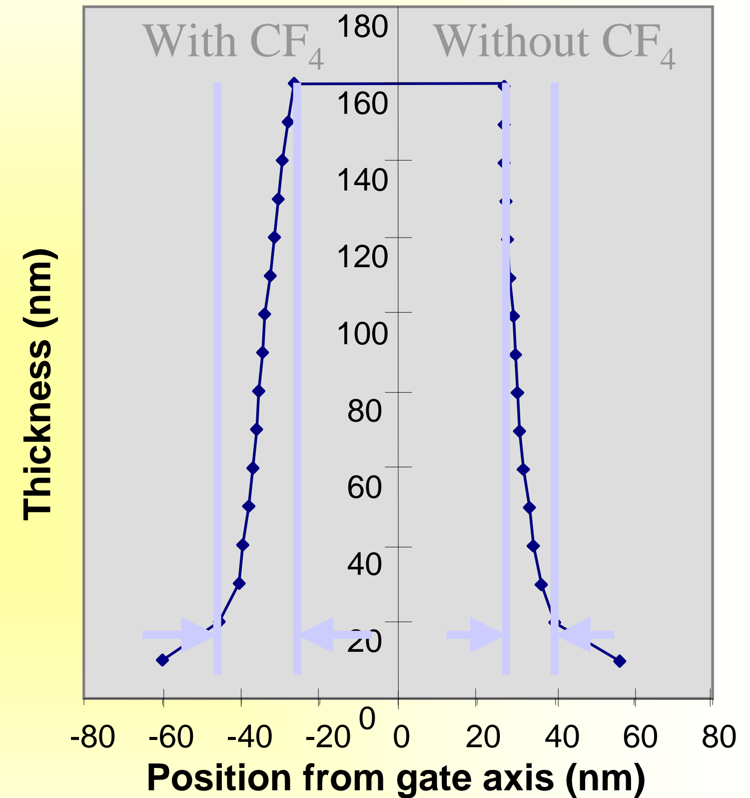
High resolution SEM: CD control of very small structures

Gate etch process

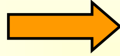


$HBr/Cl_2/O_2/CF_4$ Without CF_4



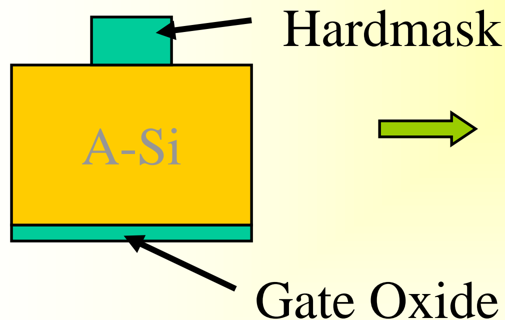


⇒ Direct correlation between passivation layer thickness and Critical Dimension of the structure

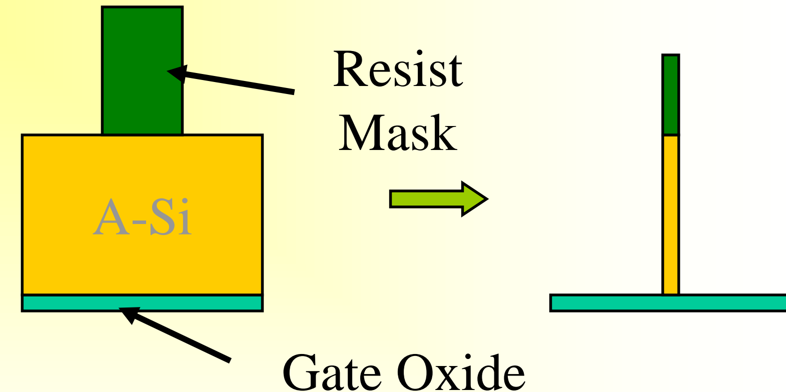
✓ Roadmap requirements  Making gate transistor always smaller than the resolution targeted for each technological node (65 nm node: gate dimension is only 45 nm)

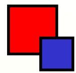
✓ Potential gate etching strategies

1- « Notched gate » approach



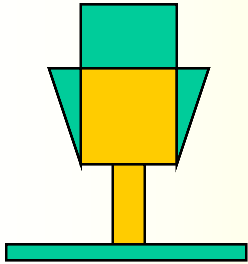
2- Resist Trimming approach



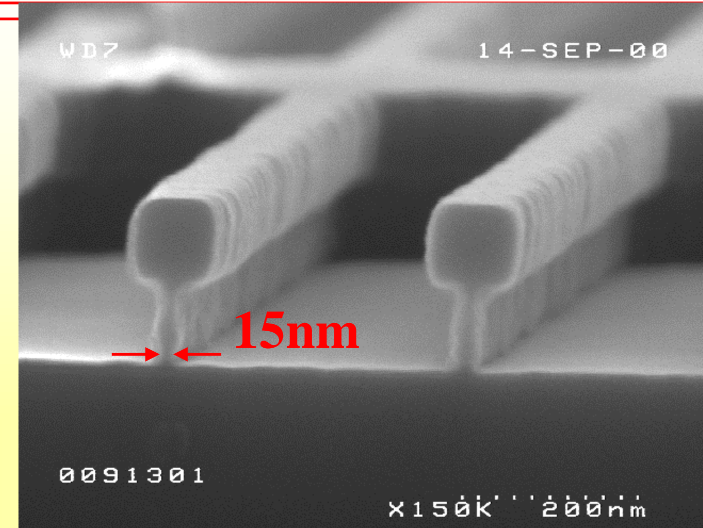


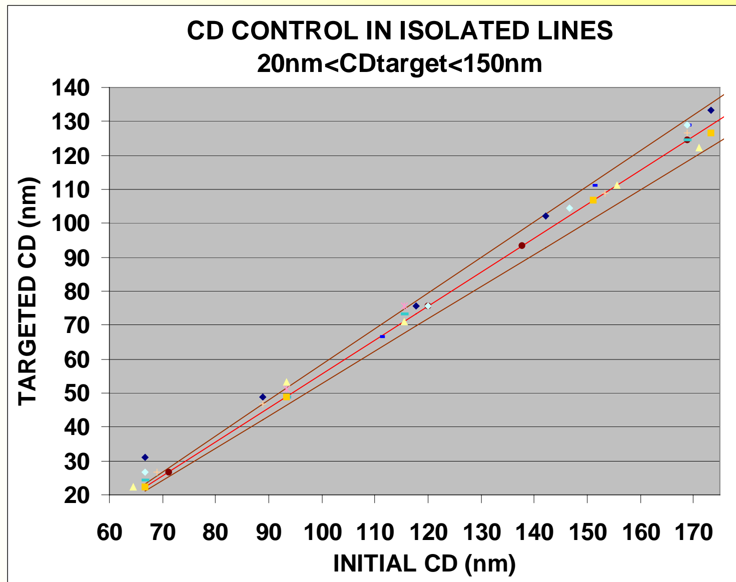
Notched gate: engineering of the passivation layer

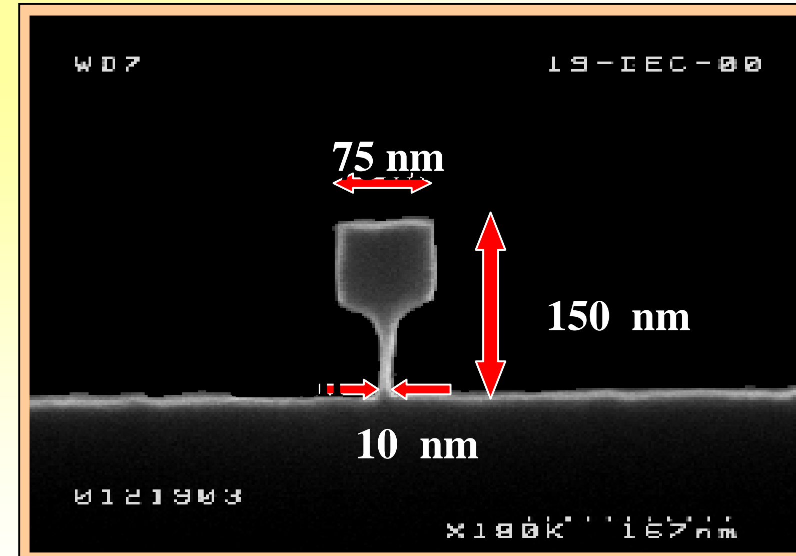
Hardmask (TEOS-HTO)

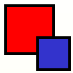


High potential of the technique to make very small gates but
1-Notch reproducibility
2-Notch uniformity



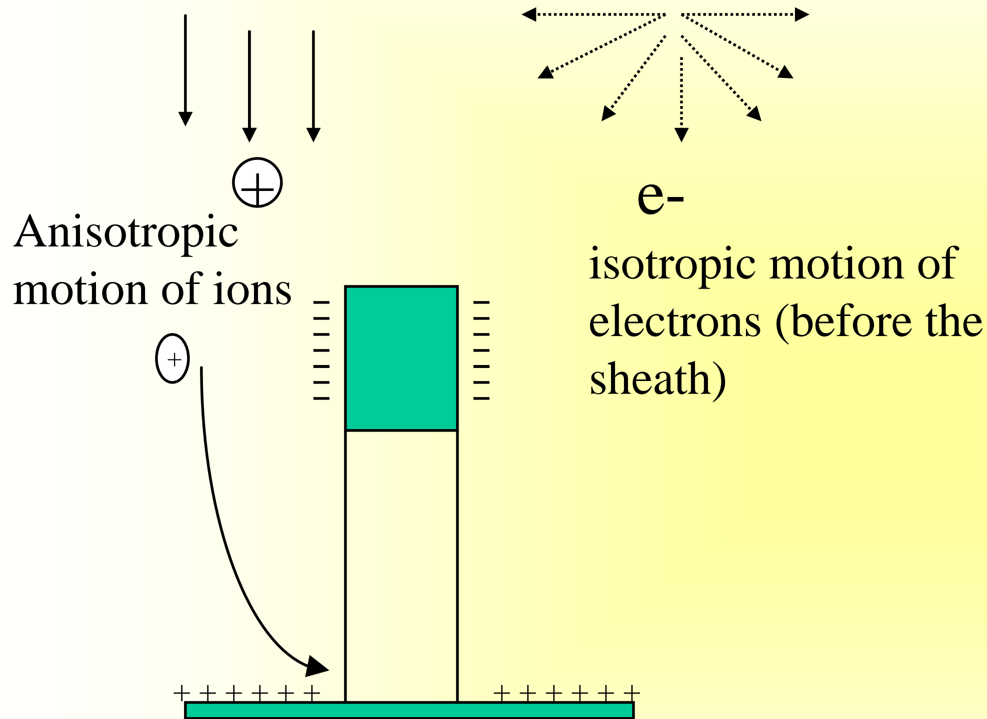


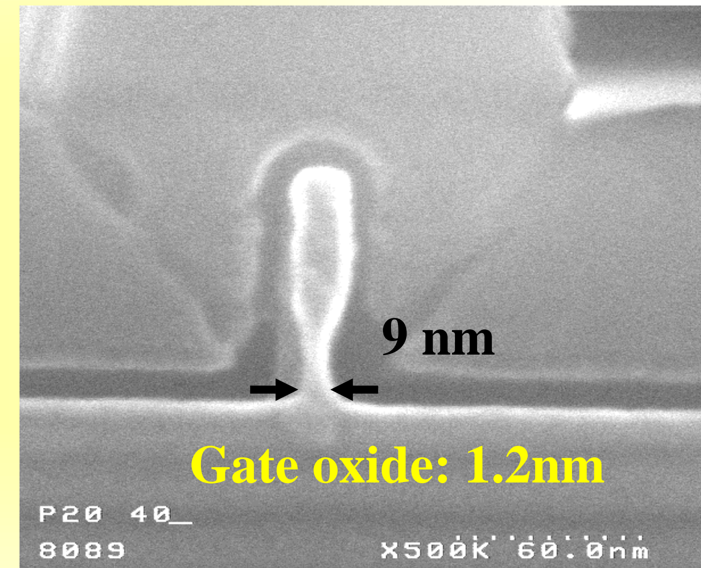




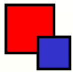
Positive charging on the gate oxide: notch control capability

Differential charging is generally considered as a problem in plasma etching: it can be used to designe a controlled « notch » at bottom of the gate

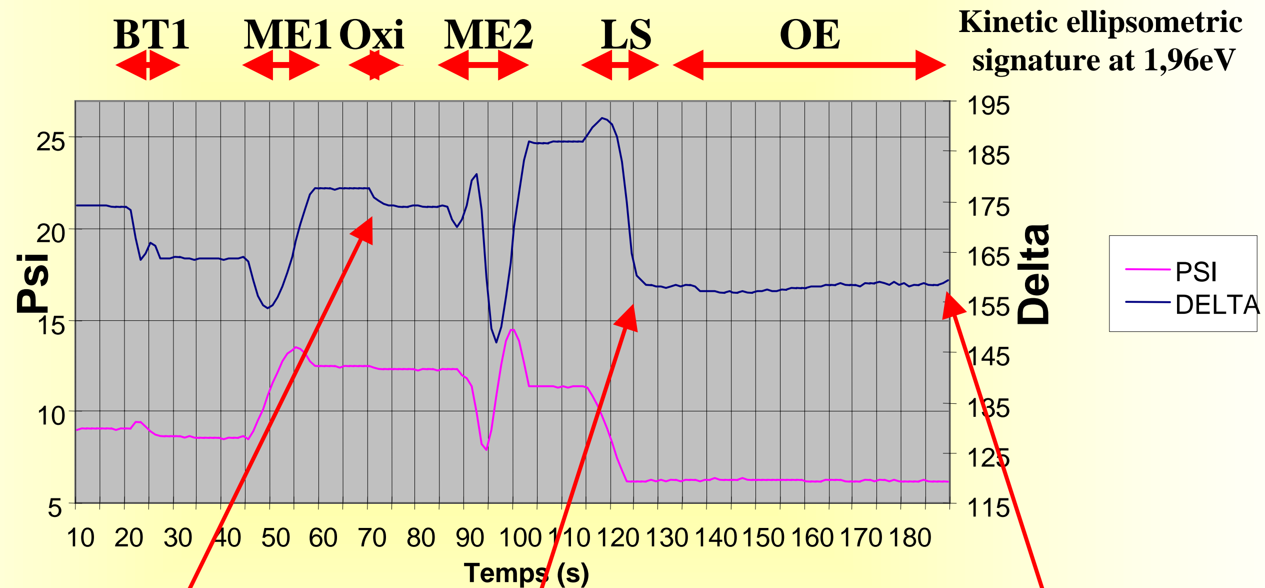


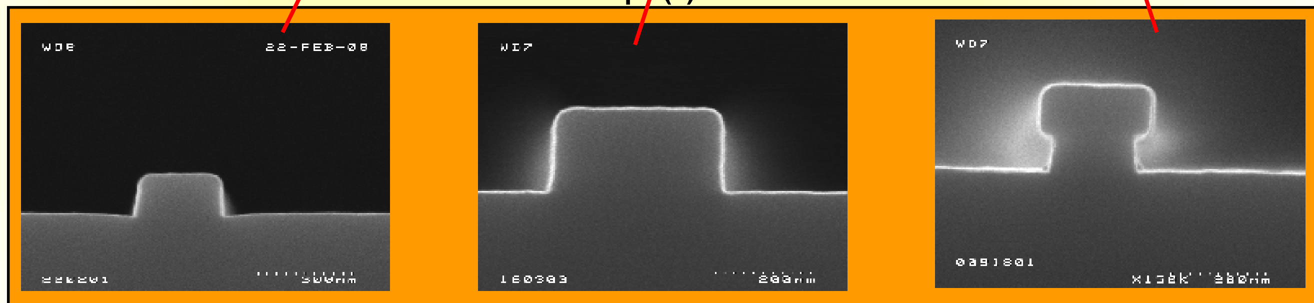


Limitations of the technique: fragility of the gate oxide

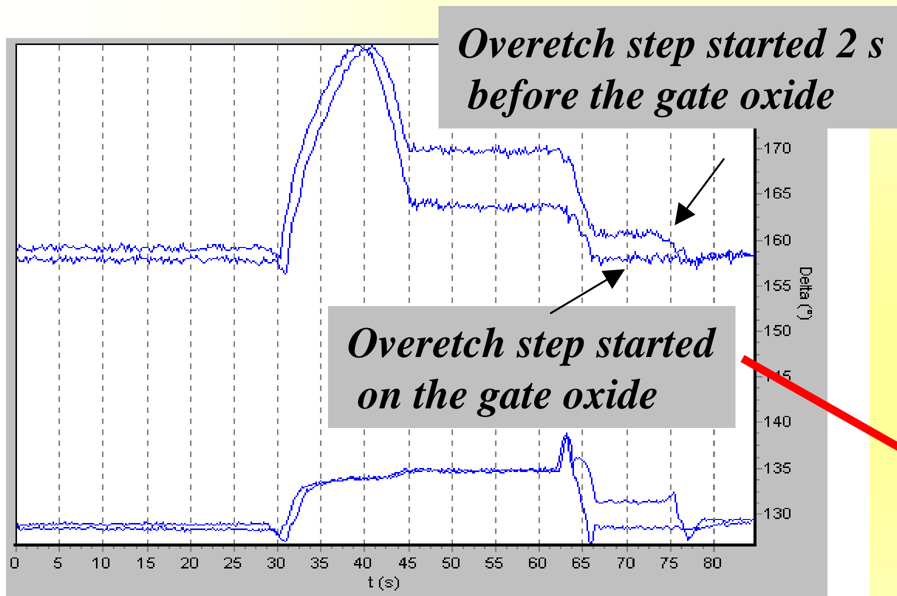


REAL TIME PROCESS MONITORING BY ELLIPSOMETRY





Real time process control : CD control capability



WD7

CD Bias (nm)

16 14 12 10 8 6 4

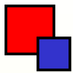
50i 75i 75d 100d

Initial Lithography

2020602 STRIP & HF

X150K 200nm

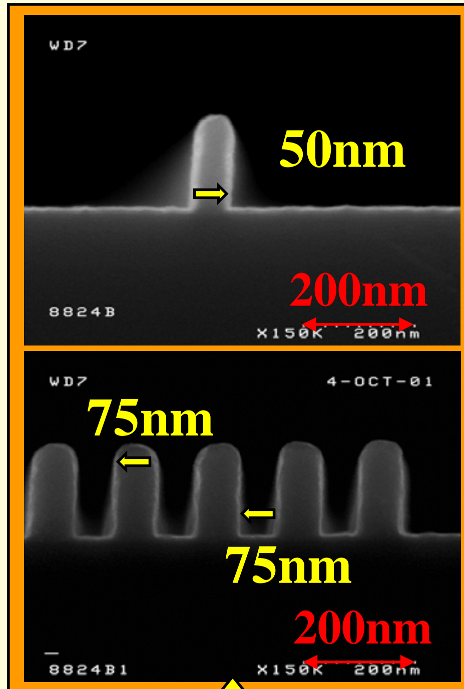
Positive charging can be used to improve CD control by polysilicon foot elimination

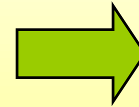


Resist trimming: the manufacturing solution

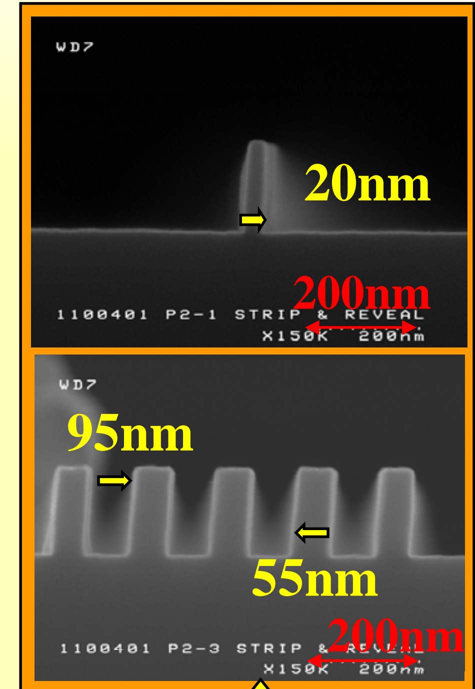
Isolated line

Nested lines



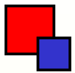


22s Trimming
+
Silicon tranfer using HBr/Cl2/O2 chemistry



Pre-etch structure

After Resist Stripping and HF cleaning

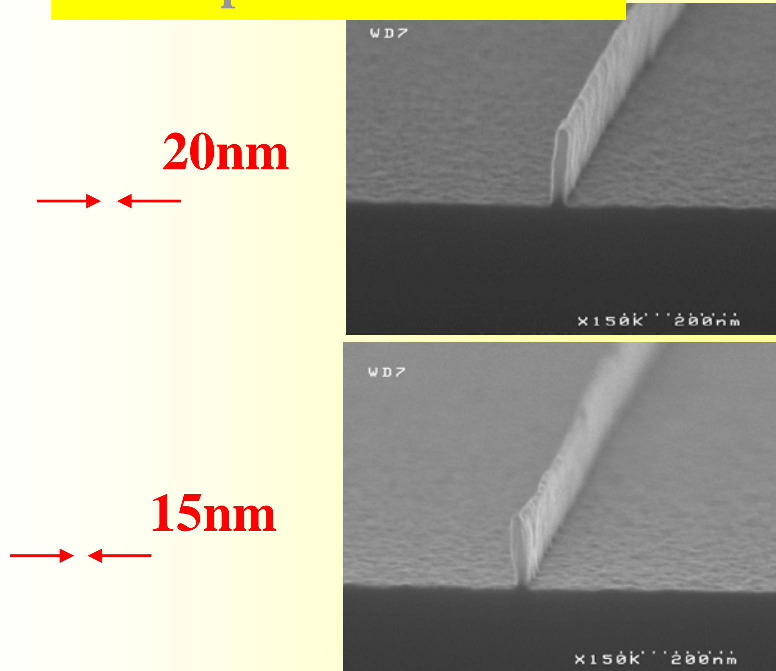


Resist trimming: limitations due to resist roughness

CD Smaller than 20nm

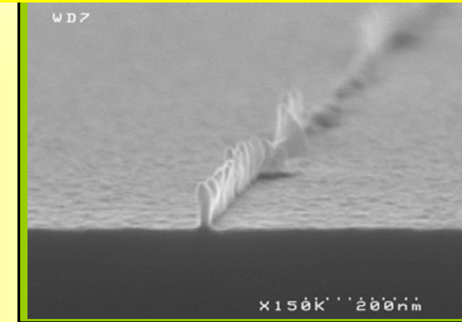
Limit 15nm

Resist profile after trim

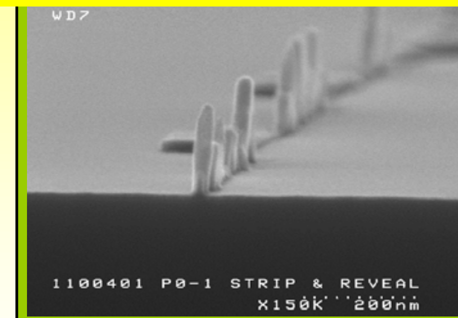


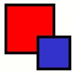
Under this limit

Resist profile after trim



Si gate profile after trim & transfer





Conclusion

<u>Keeping under control the etching of very small structures requires:</u>

-to keep the chamber walls clean using appropriate chemistries or cleaning sequences of the plasma chamber

-Investigate the layers formed on the sidewalls of any materials : they control the etch anisotropy and therefore the final dimension of the structure

-Use very sophisticated in situ and on line diagnostics to « visualize » the etching in real time

- investigating new hardwares and plasma chemistries is mandatory to move towards the limit of the top down approach