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US Patent Nr.	Title	Assignee	Filed	Date of Patent
6464843	Contamination Controlling Method and Apparatus for a Plasma Processing Chamber	LAM	8/3/99	10/15/02
6465159	Method and Apparatus for Sidewall Passivation for Organic Etch	LAM	6/28/99	10/15/02
6465309	Silicide Gate Transistors	AMD	12/12/00	10/15/02
6465836	Vertical Split Gate Effect Transistor (FET) Device	TSMC	3/29/01	10/15/02
6465841	Split Gate Flash Memory Device Having Nitride Spacer to Prevent Inter-Poly Oxide Damage	TSMC	11/13/00	10/15/02
6465847	Semiconductor -on-Insulator (SOI) Device With Hyperabrupt Source / Drain Junctions	AMD	6/11/01	10/15/02