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US Patent Nr.	Title	Assignee	Filed	Date of Patent
6506639	Method of Forming Low Resistance Reduced Channel Length Transistors	AMD	10/18/00	1/14/03
6506642	Removable Spacer Technique	AMD	12/19/01	1/14/03
6506652	Method of Recessing Spacers to Improve Salicide Resistance on Polysilicon Gates	Intel	12/9/99	1/14/03
6506687	Dry Etching Device and Method of Producing Semiconductor Devices	Hitachi	6/24/98	1/14/03
6507065	Doped Silicon Structure With Impression Image on Opposing Roughed Surfaces	Micron	6/2/01	1/14/03
6508199	Plasma Processing Apparatus	TEL	8/16/00	1/21/03
6508911	Diamond Coated Parts in a Plasma Reactor	AMAT	8/16/99	1/21/03
6509218	Front Stage Process of a Fully Depleted Silicon-on-Insulator Device	UMC	4/9/02	1/21/03
6509219	Fabrication of Notched Gates by Passivating Partially Etched Gate Sidewalls and Then Using an Isotropic Etch	IBM	8/10/01	1/21/03
6509221	Method for Forming High Performance CMOS Devices With Elevated Sidewall Spacers	IBM	11/20/00	11/26/02
6509228	Etching Procedure for Floating Gate Formation of a Flash Memory Device	UMC	8/29/00	1/21/03

6509234	Method of Fabricating an Ultra-Thin Fully Depleted SOI Device with T-shaped Gate	AMD	7/22/02	1/21/03
6509239	Method of Fabricating a Field Effect Transistor	Micron	10/28/99	1/21/03
6509241	Process for Fabricating an MOS Device Having Highly-Localized Halo Regions	IBM	12/12/00	1/21/03
6509263	Method for Fabricating a Semiconductor Memory Device Having Polysilicon With an Enhanced Surface Concentration and Reduced Contact Resistance	SAMSUNG	11/14/00	1/21/03
6509542	Voltage Control Sensor and Control Interface for Radio Frequency Power Regulation in a Plasma Reactor	LAM	4/25/00	1/21/03
6509611	Method for Wrapped-Gate MOSFET	IBM	9/21/01	1/21/03
6509618	Device Having Thin First Spacers and Partially Recessed Thick Second Spacers for Improved Salicide Resistance on Polysilicon Gates	Intel	1/4/00	1/21/03