

Vol. 3: January 2003

US Patent Nr.	Title	Assignee	Filed	Date of Patent
6489206	Method for Forming Self-Aligned Local-Halo Metal-Oxide-Semiconductor Device	UMC	3/22/01	12/3/02
6485572	Use of Pulsed-Grounding Source in a Plasma Reactor	Micron	8/28/00	11/26/02
6485602	Plasma Processing Apparatus	TEL	7/18/01	11/26/02
6485990	Feed-Forward Control of an Etch Processing Tool	AMD	1/4/00	11/26/02
6486067	Method for Improving the Electrical Isolation Between the Contact and Gate in a Self-Aligned Contact MOSFET Device Structure	TSMC	10/29/99	11/26/02
6486070	Ultra-High Oxide to Photoresist Selective Etch of High-Aspect-Ratio Openings in Low-Pressure, High-Density Plasma	LAM	9/21/00	11/26/02
6486492	Integrated Critical Dimension Control for Semiconductor Device Manufacturing	AMAT	11/20/00	11/26/02
6486496	Polysilicon Thin Film Transistor Structure	UMC	11/26/01	11/26/02
6486518	Structures and Method With Bitline Self-Aligned to Vertical Connection	TI	9/29/99	11/26/02
6486520	Structure and Method for a Large-Permittivity Gate Using a Germanium Layer	TI	4/10/01	11/26/02
6488807	Magnetic Confinement in a Plasma Reactor Having an RF Bias Electrode	AMAT	5/3/00	12/3/02

6488863	Plasma Etching Method	TEL	10/5/01	12/3/02
6489207	Method of Doping a Gate and Creating a Very Shallow Source/Drain Extension and Resulting Semiconductor	IBM	6/1/201	12/3/02
6489237	Method of Patterning Lines in Semiconductor Devices	TSMC	12/4/01	12/3/02
6489245	Methods for Reducing Mask Erosion During Plasma Etching	LAM	7/5/00	12/3/02
6489248	Method and Apparatus for Etch Passivating and Etching a Substrate	AMAT	8/23/02	12/3/02